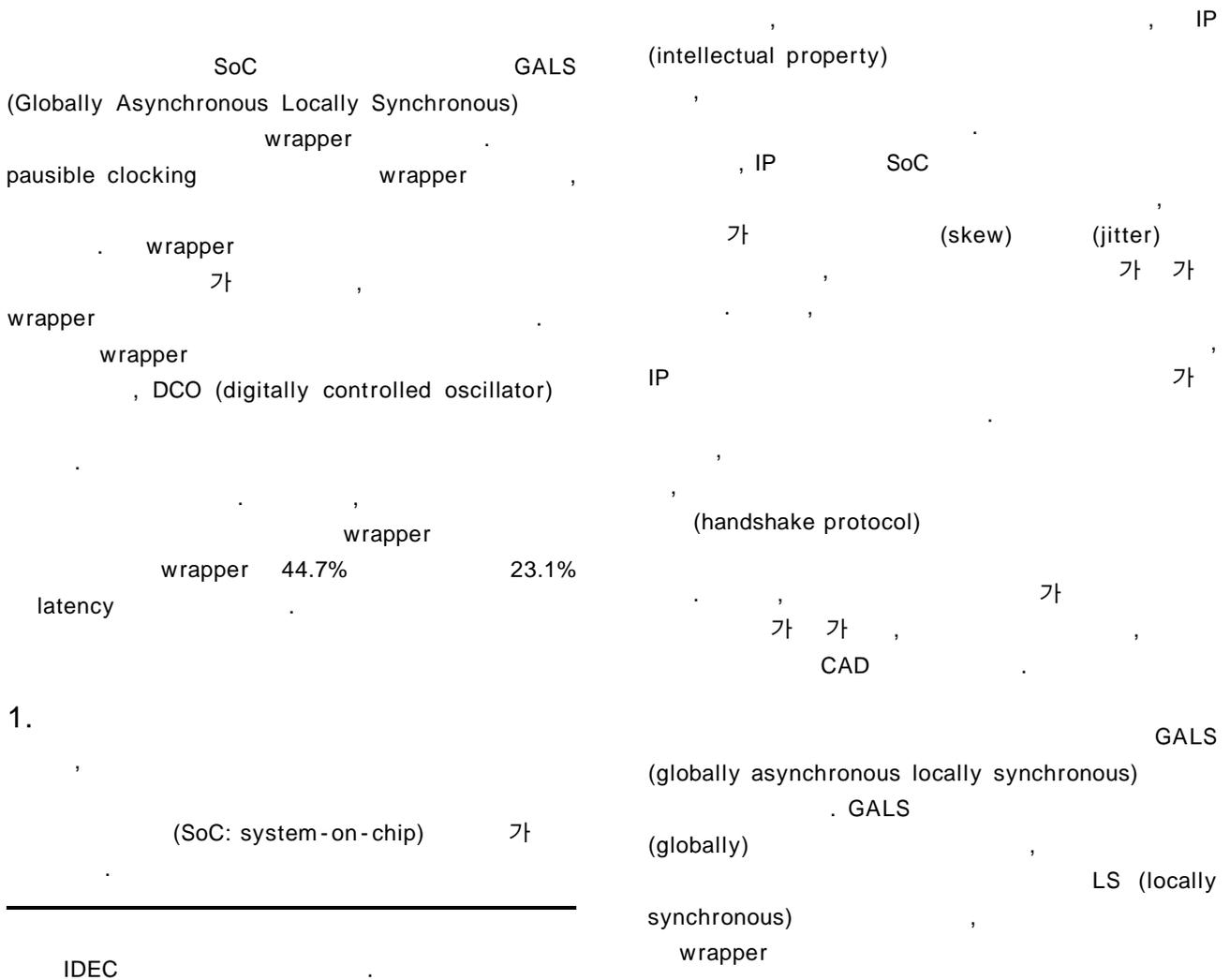


GALS (Globally Asynchronous Locally Synchronous) Decoupled Wrapper

An Efficient Implementation of a Decoupled Wrapper for GALS Systems

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GALS

가 , IP 가 IP

가 ,

GALS

[2] PCC(Pausible Clocking Control)가 , PCC

2 가

[3] [4]

wrapper PCC

wrapper가 [7][8]. latency가

wrapper

. Wrapper , DCO

2. Wrapper

wrapper decoupled wrapper [8]

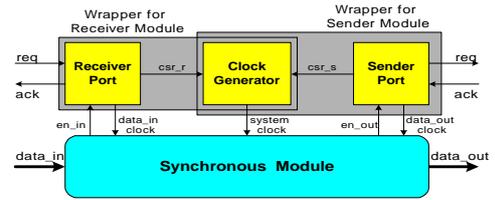
latency,

2.1. Wrapper

1 wrapper

(Sender Module) , (Receiver Module)

(Port) , pausable (Clock Generator) 가



1 wrapper

(rec_en, sen_en) wrapper , (csr:clock stop req)

(data_clk)

[7][8] normal

decoupled wrapper

2.2. Normal /

2 AFSM normal

[4].

csr

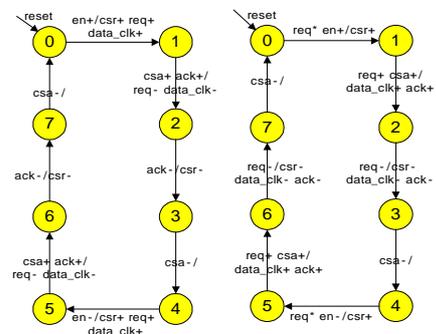
AFSM(asynchronous finite state machine)

Mealy

AFSM burst-mode

가

가

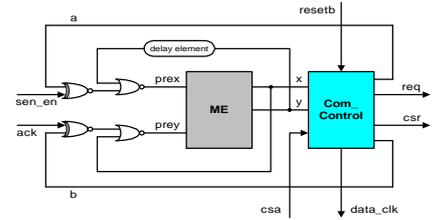


(a) 2 Normal

(b) AFSM (a) AFSM (b)

, decoupled normal

[8]



3 wrapper decoupled

2.3. Decoupled wrapper

2.3.1. Decoupled

4

sen_en

(1)

sen_en+ req+ ack+ req- ack- sen_en- req+...
 -- clock stop -- (1)

2.3.2. decoupled wrapper

[7] decoupled

, LS

가

req+ sen_en
 ack- sen_en
 가

AFSM
 가 가

sen_en+ req+ ack+ req- ack- sen_en- req+...
 - clock no stop - (2)

sen_en+ req+ sen_en- ack+ req- ack- req+...
 - clock stop - (3)

sen_en+ req+ ack+ req- sen_en- ack- req+...
 clock stop --- (4)

decoupled wrapper가 decoupled

[8]. 3

wrapper

AFSM

ME-element

, 2 (

phase)

4

feedback

a, b

com_control

4

com_control

AFSM

normal

가

(2) sen_en

sen_en 가

(3) (4)

sen_en

,
 가

. ack-

sen_en

req+

ack

sen_en

,
 가

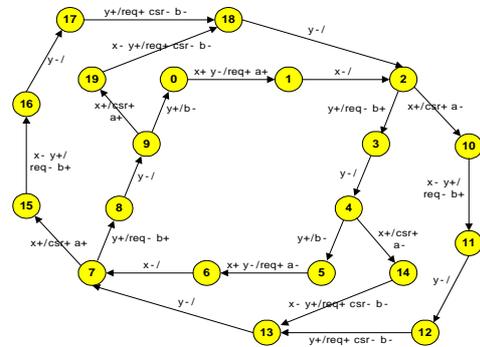
가

, (sen_en+, ack+), (sen_en+, ack-),

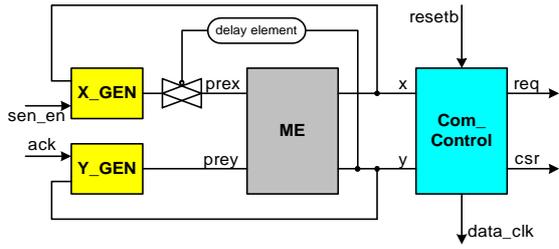
(sen_en-, ack+), (sen_en-, ack-) 4

가

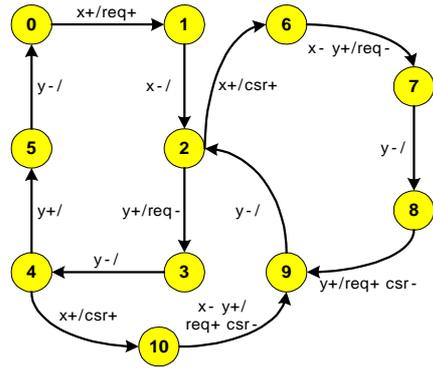
가



4 wrapper Com_Control AFSM



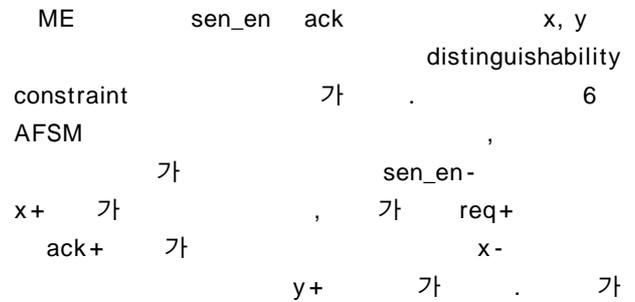
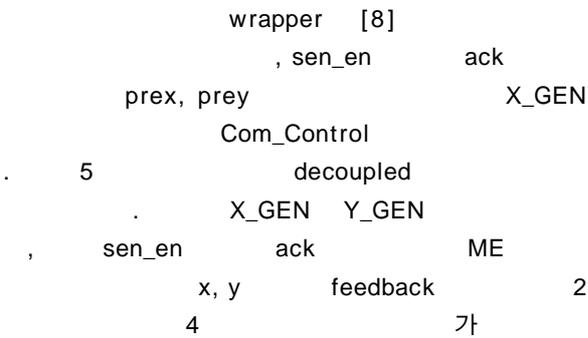
5 decoupled wrapper



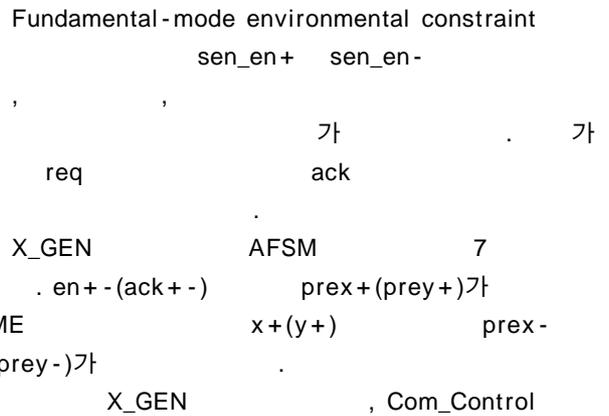
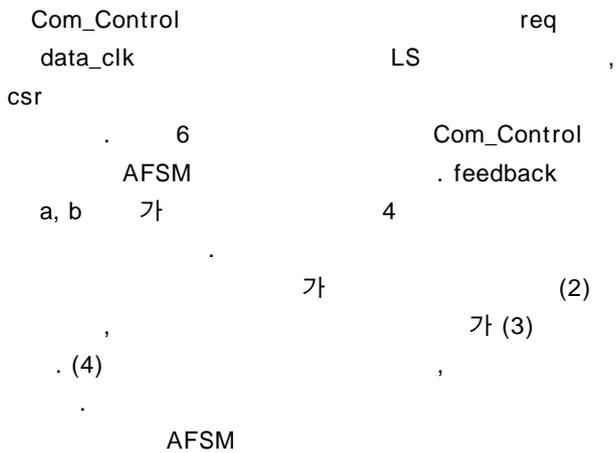
6 decoupled wrapper Com_control AFSM

2.4. decoupled wrapper

2.4.1.



2.4.2. Com_Control

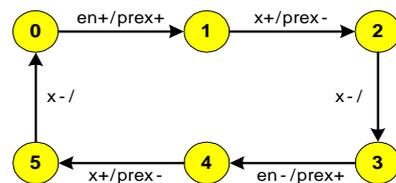


[10].

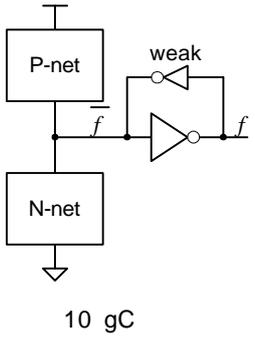
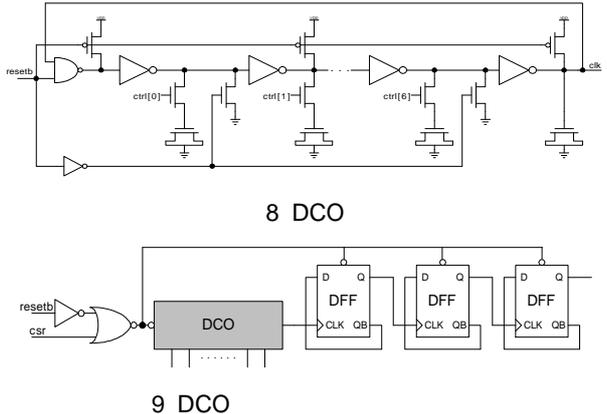
fundamental-mode environmental constraint :

가 가

distinguishability constraint :



7 X_GEN AFSM



2.4.3. DCO

GALS

(inverter chain)

[1]

가

가

가

[6].

8 DCO

(digitally controlled oscillator)[5]

DCO

(9)

40MHz~300MHz

resolution

3. Wrapper

2.2 normal

decoupled

AFSM

busrt-mode

3D[9]

3D

set, reset

10

gC(generalized

C-element)[10]

set, reset

N-net

P-net

decoupled

0.35 μm

3D

GALS

)

wrapper

GALS

2

4.74ns,

0.51ns

[8]

40.75%, 67.3%

1

[8]

wrapper

wrapper

		(100MHz)
dec[8]	8.02 ns	3.60mW
	4.74 ns	3.65nW

1

wrapper

gC

HSpice

, throughput

2- AND-OR

ModelSim



11 [8]

(a)

(b)

	Gate level (AO)		TR level (gC)	
	Area	Latency	Area	Latency
dec[8]	307	1.73ns	416	1.43ns
	228	1.30ns	230	1.10ns
	25.7%	24.8%	44.7%	23.1%

2 Area latency

11 [8] (a) ,
(b)
(a) feedback
a, b ,
latency가 (b)

2 [8] decoupled wrapper
wrapper
latency
, 44.7%,
latency 23.1%

throughput 3 normal
GALS [8]
wrapper가 [8]
latency
가

	5	10	25	50	100	250
dec[8]	9.712	9.381	10.277	9.887	9.588	9.735
	9.713	9.383	10.282	9.896	9.605	9.867

3 Normal (%)

4. wrapper ,
,
pausable clocking
wrapper
,
wrapper 44.7%
latency
DCO

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